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CENTRAL FAX CENTER****NOV 13 2006****M-15281US
10/753,673****IN THE CLAIMS**

The following is a complete listing of the pending claims:

1. (previously presented) A two-transistor PMOS memory cell, comprising:
a PMOS select transistor having a drain and a source formed as separate P+ diffusion regions in an N- well;
a PMOS floating gate transistor having a drain and a source formed as separate P+ diffusion regions in the N-well, wherein the P+ diffusion region that forms the floating gate transistor's drain is the same P+ diffusion region that forms the select gate transistor's source;
and
an N implant underlying only the P+ diffusion region that forms the floating gate transistor's drain such that an N implant does not underlie either of the P+ diffusion regions forming the select gate' transistor drain and the floating gate's transistor's source, and wherein a lateral extent of the N implant is substantially the same as a lateral extent of the P+ diffusion region that forms the floating gate transistor's drain.
2. (cancelled)
3. (currently amended) The two-transistor PMOS memory cell of claim 1, wherein the drain of the PMOS select transistor couples to a bit line of a memory array, and wherein a select gate of the PMOS select transistor couples to a word line of the memory array.
4. (currently amended) The two-transistor PMOS memory cell of claim 1, wherein a floating gate of the PMOS floating gate transistor is formed in a first polysilicon layer, and

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M-15281US

10/753,673

wherein a control gate of the PMOS floating gate transistor is formed in a second polysilicon layer.

5. (currently amended) The two-transistor PMOS memory cell of claim 1 2, wherein the memory cell includes a single polysilicon layer containing a floating gate of the PMOS floating gate transistor, and wherein a control gate of the PMOS floating gate transistor is formed as a P+ diffusion region in the N- well.

6. (currently amended) The two-transistor PMOS memory cell of claim 1 2, wherein the memory cell is configured such that the floating gate transistor may be programmed using band-to-band tunneling.

7. (currently amended) The two-transistor PMOS memory cell of claim 1 2, wherein the memory cell is configured such that the floating gate transistor may be programmed using Fowler Nordheim tunneling.

8. (currently amended) The two-transistor PMOS memory cell of claim 1 2, wherein the P+ diffusion region that forms the floating gate transistor's drain has a thickness of approximately 0.1 to 0.25 microns.

9. (currently amended) The two-transistor PMOS memory cell of claim 1 2, wherein the thickness of the N implant underlying the P+ diffusion region that forms the floating gate transistor's drain is approximately 0.1 to 0.25 microns.

10. (withdrawn)

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11. (withdrawn)
12. (withdrawn)
13. (withdrawn)
14. (withdrawn)

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